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(71) Applicant : **SONY CORPORATION**
7-35 Kitashinagawa 6-chome Shinagawa-ku
Tokyo 141 (JP)

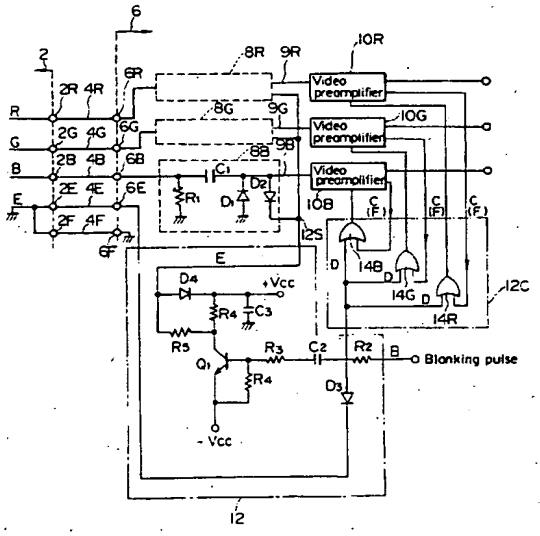
(72) Inventor : **Okamoto, Nobuyuki**
c/o Sony Corporation, 7-35 Kitashinagawa 6-chome
Shinagawa-ku, Tokyo (JP)

(74) Representative : **Nicholls, Michael John et al**
J.A. Kemp & Co., 14, South Square, Gray's Inn
London WC1R 5LX (GB)

(54) Display device testing circuit.

(57) A display device testing circuit comprising a false video signal generator for producing a false video signal from a blanking pulse of the display device in a state where none of signal cables is connected to an input terminal, and supplying such false video signal to the video amplifier; and a false clamp pulse generating circuit for producing a false clamp pulse from the blanking pulse and supplying such false clamp pulse to a pedestal clamper in the video amplifier, thereby realizing a simplified test of the video amplifier at low cost.

FIG. 1



EP 0 496 580 A2

The present invention relates to a circuit for testing a display device to detect any fault therein.

It has been known heretofore that, for the purpose of detecting the presence or absence of any fault in a CRT display device when no video signal is supplied from a computer, a test is conducted to brighten the CRT by either lowering a cathode voltage to the CRT or raising a first grid voltage therein.

The above prior art is effective for checking if a deflector and a power supply in the display device are normal or not. However, it is not exactly effective for testing a video amplifier which is incorporated to amplify a video signal. Although there is avaiable an improved display device of a type including a signal generator to test a video amplifier, a problem of high production cost is unavoidable.

It is an object of the present invention to provide a display device testing circuit which is capable of testing a video amplifier in a display device at low cost.

Another object of the present invention resides in providing a display device testing circuit of a simplified constitution capable of detecting any fault in both a video amplifier and a pedestal clamper incorporated in the display device for clamping a video signal to a pedestal level by a clamp pulse produced from the video signal.

According to the present invention there is provided a circuit for testing a display device equipped with a video amplifier to amplify a video signal, the circuit comprising a false video signal generator for producing a false video signal from a blanking pulse of the display device in a state where none of signal cables is connected to an input terminal, and supplying such false video signal to the video amplifier.

Hence, a false video signal produced from a blanking pulse is supplied to the video amplifier, which can thereby be tested without the necessity of providing any additional signal generator.

For cases where a video amplifier includes a clamper for producing a clamp pulse from said video signal and clamping said video signal to a predetermined level by said clamp pulse, preferably said circuit further comprising:

a false clamp pulse generating circuit for producing a false clamp pulse from said blanking pulse and supplying the false clamp signal to said clamper.

Hence, a false video signal produced from a blanking pulse is supplied to the video amplifier while a false clamp pulse produced from the blanking pulse is supplied to the pedestal clamper, so that there never occurs a state where the original level (e.g., white level) of the false video signal is clamped to a different level (e.g., black level), hence achieving a simplified correct test of the video amplifier equipped with the pedestal clamper.

According to the present invention, there is provided a method for testing a display device equipped with a video amplifier to amplify a video signal, said method comprising the steps of producing a false video signal from a blanking pulse of said display device in a state where no signal cables are connected to an input terminal, and supplying such false video signal to said video amplifier.

The present invention will be more clearly understood from the following description given by way of example only with reference to the accompanying drawings in which:

Fig.1 is a circuit diagram of an exemplary embodiment representing the display device testing circuit of the present invention; and

Fig. 2 is a waveform timing chart of signals obtained in principal portions of the display device testing circuit shown in Fig. 1.

Fig. 1 is a circuit diagram of an exemplary embodiment which represents the display device testing circuit of the present invention. A red signal input terminal 6R, a green signal input terminal 6G, a blue signal input terminal 6B and ground terminals 6E, 6F of a display device 6 are connected via cables 4R, 4G, 4B and 4E, 4F respectively to output terminals 2R, 2G, 2B and ground terminals 2E, 2F for a red signal (R), a green signal (G) and a blue signal (B) of a primary color video image supplied from a computer 2 which serves as a signal source. The red, green and blue input terminals 6R, 6G and 6B are connected respectively to input circuits 8R, 8G and 8B. The three input circuits 8R, 8G and 8B are mutually the same in structure, and each has an input resistor R1 connected between the input terminal (6B, 6G or 6B) and the ground point, a capacitor C1 connected between the input terminal and an output line (9R, 9G or 9B), a static protection diode D1 whose cathode is connected to the output line and whose anode is connected to the ground point, and a static protection diode D2 whose anode is connected to the output line and whose cathode is connected to an output line 12S of an undermentioned false video signal generator 12.

The static protection diode D1 is turned on when a negative pulse voltage lower than the ground potential is supplied to the input terminal (6R, 6G or 6B), and serves to prevent generation of any voltage lower than the ground potential at the output line (9R, 9G or 9B). Meanwhile the static protection diode D2 is turned on when a positive pulse voltage higher than a predetermined voltage (in this embodiment, a bias voltage +Vcc of an undermentioned false video signal generator 12) is supplied to the input terminal (6R, 6G or 6B), and serves to prevent generation of any voltage higher than the predetermined voltage at the output line (9R, 9G or 9B).

The output lines 9R, 9G and 9B of the input circuits 8R, 8G and 8B are connected respectively to input terminals of video preamplifiers 10R, 10G and 10B. The video preamplifiers 10R, 10G and 10B are mutually the same in structure with a function of

amplifying a video signal, and each includes a pedestal clamper for clamping a back porch of the video signal to a pedestal level by a clamp pulse C produced from the video signal.

The clamp pulses C produced from the video preamplifiers 10R, 10G and 10B by delaying a sync signal obtained from a sync separator are supplied via OR gates 14R, 14G and 14B respectively to the pedestal clampers in the video preamplifiers 10R, 10G and 10B.

The false video signal generator 12 produces a false video signal, which is a false maximum-white signal E, out of the blanking pulse B received from a deflector and then supplies such false video signal via the output line 12S to cathodes of the static protection diodes D2 in the input circuits 8R, 8G and 8B. Furthermore the false video signal generator 12 includes a false clamp pulse generating circuit 12C which produces a false clamp pulse D out of the blanking pulse B obtained from the deflector and supplies such false clamp pulse D via OR gates 14R, 14G and 14B to the pedestal clampers in the video preamplifiers 10R, 10G and 10B.

More specifically, the false video signal generator 12 comprises a series input resistor R2 to receive the blanking pulse B, a capacitor C2 and a resistor R3 connected in series to the resistor R2, an inverter transistor Q1 whose base is connected to the resistor R3, a resistor R4 connected between the base and the emitter of the transistor Q1, a negative voltage souece -Vcc for biasing the emitter of the transistor Q1, a resistor R4 connected between the collector of the transistor Q1 and the positive bias voltage source +Vcc, a capacitor C3 connected between the positive bias voltage source +Vcc and the ground point, a capacitor C3 connected between the positive bias voltage source +Vcc and the ground point, a resistor R5 connected between the collector of the transistor Q1 and the output line 12S, a diode D4 whose cathode is connected to the positive bias voltage source +Vcc and whose anode is connected to the output line 12S, and a diode D3 whose anode is connected to the junction of the resistor R2 and the capacitor C2 and whose cathode is connected to the ground terminal 6E. The false clamp pulse generating circuit 12C consists of a signal line which connects the junction of the resistor R2 and the capacitor C2 to the inputs of the OR gates 14R, 14G and 14B.

Fig. 2 shows exemplary waveforms of signals obtained in principal portions of the embodiment representing the display device testing circuit shown in Fig. 1. The operation of the testing circuit in Fig. 1 will now be described below with reference to Fig. 2. In a normal operating state, the output terminals 2R, 2G, 2B and the ground terminal 2E of the computer 2 are connected via the cables 4R, 4G, 4B respectively to the input terminals 6R, 6G and 6B of the display device 2. When the blanking pulse B is supplied in this state to the false video signal generator 12, the diode D3 is turned on so that the potential at the junction of the resistor R2 and the capacitor C2 is held to be constant (at the ground potential), whereby the false maximum-white signal E is not generated in the output line 12S, and the false clamp pulse D is not generated either from the false clamp pulse generating circuit 12C.

The pedestal clampers in the video preamplifiers 10R, 10G and 10B produce clamp pulses C in synchronism with the trailing edges of sync pulses of the video signal A supplied from the input circuits 8R, 8G and 8B respectively, and the video signal is clamped to the pedestal level in response to the pulses C received via the OR gates 14R, 14G and 14B respectively.

If the blanking pulse B is supplied to the false video signal generator 12 when the input terminals 6R, 6G, 6B and the ground terminal 6E of the display device 2 are not connected respectively to the output terminals 2R, 2G, 2B and the ground terminal 2E of the computer 2, then the diode D3 is maintained in its off-state since the ground terminal 6E is not connected to the ground terminal 2E, whereby the blanking pulse B is inverted and amplified by the inverter transistor Q1 and a false maximum-white signal E is generated in the output line 12S. The false clamp pulse generating circuit 12C regards the input blanking pulse B as a false clamp pulse D and supplies the same via the OR gates 14R, 14G and 14B respectively to the pedestal clampers in the video preamplifiers 10R, 10G and 10B.

The pedestal clampers in the video preamplifiers 10R, 10G and 10B clamp the black level of the false maximum-white signal E to the pedestal level (black level) by using the false clamp pulse D. Consequently the white level of the false maximum-white signal E can be maintained directly as the white level.

If a clamp pulse F is generated in synchronism with the leading edge of the false maximum-white signal E by the pedestal clampers in the video preamplifiers 10R, 10G and 10B without the provision of the false clamp pulse generating circuit 12C, the white level of the false maximum-white signal is clamped to the pedestal level (black level) since the timing of generation of the clamp pulse F corresponds to the white level of the false maximum-white signal E, so that the false maximum-white signal E fails to be maximum white. It becomes therefore necessary to provide the circuit 12C which is capable of generating the false clamp pulse 2D synchronously with the false maximum-white signal E.

In the embodiment mentioned, an inverter transistor is employed to generate a false maximum-white signal. However, it is obvious that any other suitable electronic element may be used as well.

Although in the embodiment a false maximum-white signal is generated to serve as a false video sig-

nal, it is also possible to generate a false red signal, green signal or the like for the same purpose. However, the use of a false maximum-white signal is the most preferable since it is adapted for testing all of the red, green and blue video preamplifiers simultaneously.

Hence, a false video signal is produced from a blanking pulse and then is supplied to a video amplifier, so that the video amplifier can be tested by a minimum number of additional component elements.

Further, a false clamp pulse is produced from a blanking pulse and then is supplied to a pedestal clamper, so that the black level, for example, of a false video signal can be clamped properly to the pedestal black level, hence realizing a simplified correct test of the video amplifier equipped with the pedestal clamper.

Claims

1. A circuit for testing a display device equipped with a video amplifier to amplify a video signal, said circuit comprising:

   a false video signal generator for producing a false video signal from a blanking pulse of said display device in a state where no signal cables are connected to an input terminal, and supplying such false video signal to said video amplifier.

2. A circuit according to claim 1 for testing a display device equipped with a video amplifier including a clamper for producing a clamp pulse from said video signal and clamping said video signal to a predetermined level by said clamp pulse, said circuit further comprising:

   a false clamp pulse generating circuit for producing a false clamp pulse from said blanking pulse and supplying the false clamp signal to said clamper.

3. A method for testing a display device equipped with a video amplifier to amplify a video signal, said method comprising the steps of producing a false video signal from a blanking pulse of said display device in a state where no signal cables are connected to an input terminal, and supplying such false video signal to said video amplifier.

4. A method according to claim 3 for testing a display device equipped with a video amplifier including a clamper for producing a clamp pulse from said video signal and clamping said video signal to a predetermined level by said clamp pulse, said method further comprising the steps of producing a false clamp pulse from said blanking pulse and supplying the false clamp signal to said clamper.

FIG. 1

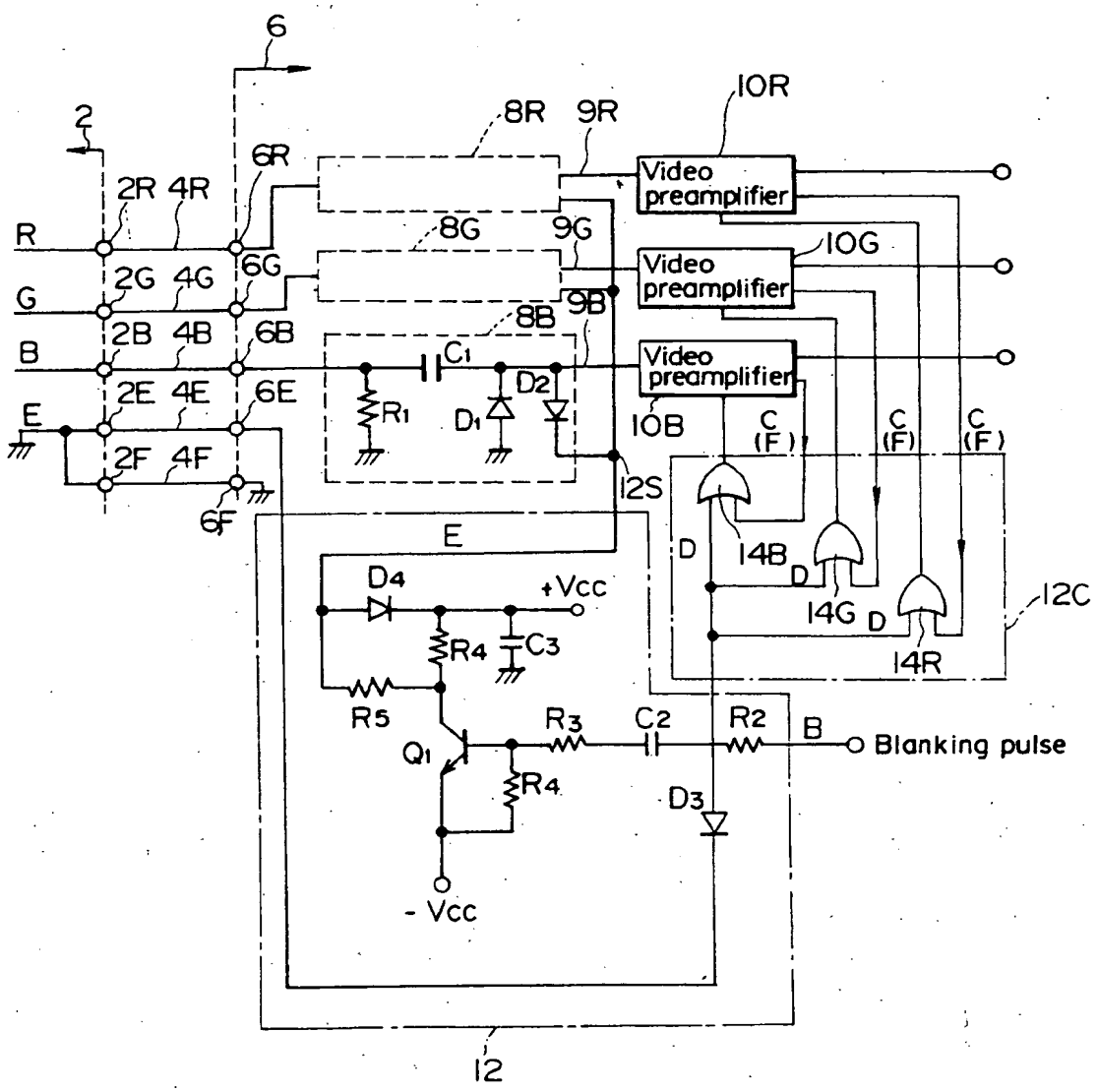

6
2
8R
9R
10R
6R
2R 4R
R
Video preamplifier
8G
9G
10G
6G
2G 4G
G
Video preamplifier
8B
9B
6B
2B 4B
B
C1
D2
Video preamplifier
R1
D1
10B
C (F)
C (F)
C (F)
2E 4E
6E
E
2F 4F
6F
12S
E
D
14B
D
14G
D
14R
12C
D4
+Vcc
R4
C3
R5
R3
C2
R2
B
Blanking pulse
Q1
R4
D3
- Vcc
12

FIG. 2A

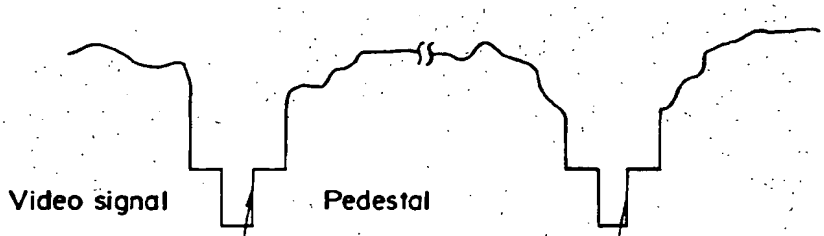


FIG. 2B

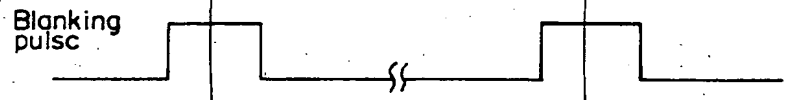


FIG. 2C

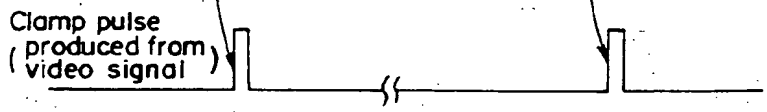


FIG. 2D

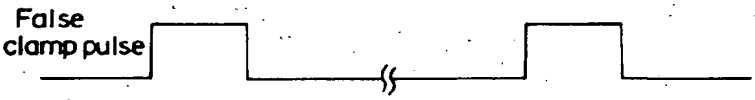


FIG. 2E

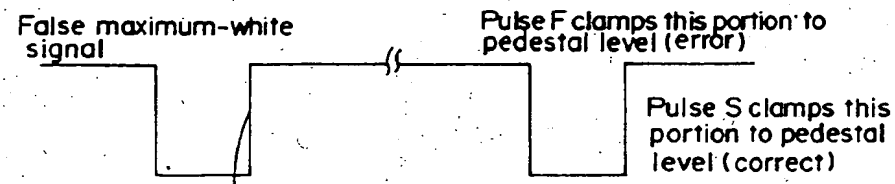


FIG. 2F